12. The apparatus of claim 14, wherein said processor reads decompressed texture data contained in said texture buffer and performs image processing of said decompressed texture data for conversion to image data.

13. The apparatus of claim 14, wherein said processor reads compressed texture data from said first storage device, said data decompression circuit decompresses said read compressed texture data, and said processor stores said decompressed texture data in said texture buffer.

14. An apparatus for image processing, comprising:

a processor including a data decompression circuit;

a first storage device having texture data and electronically coupled to said processor; and

a texture buffer having decompressed texture data and electrically coupled to said processor; wherein

transmission of texture data between said texture buffer and said processor is faster than transmission of texture data between said storage device and said processor.

15. An apparatus for image processing, comprising:

a processor including a data decompression circuit;

a first storage device having texture data and electronically coupled to said processor;

a texture buffer having decompressed texture data and electrically coupled to said processor; and

a first data bus and a second data bus, wherein said first data bus carries texture data between said texture buffer and said processor faster than said second data bus carries texture data from said storage device and said processor.

Please add the following new claims 27-34:

27. The apparatus of claim 15, further comprising a frame buffer, wherein said processor stores image data in said frame buffer.

28. The apparatus of claim 15, wherein said processor reads decompressed texture data contained in said texture buffer and performs image processing of said decompressed texture data for conversion to image data.

29. The apparatus of claim 15, wherein said processor reads compressed texture data from said first storage device, said data decompression circuit decompresses said read compressed texture data, and said processor stores said decompressed texture data in said texture buffer.

30. The apparatus of claim 29, wherein said processor includes a FIFO storage device which temporarily stores said read compressed texture data.

31. The apparatus of claim 30, wherein said data decompression circuit receives said read compressed texture data from said FIFO storage device.

32. The apparatus of claim 29, wherein said processor includes a palette transformation circuit, said palette transformation circuit performing palette transformation of said decompressed texture data.

33. The apparatus of claim 29, wherein said processor includes a mip map generation circuit, said mip map generation circuit generating a mip map of said decompressed texture data.

34. The apparatus of claim 15, wherein said texture data in said first storage device is compressed.